REMARKS

I. Pending Claims

Claims 1-18 were pending in the application as originally filed. Claims 1, 9 and 16 have been cancelled. Claims 19-24 are being added in this response. Therefore, Claim 2-8, 10-15, and 17-24 are pending after entry of this response. Based upon the remarks below, allowance of the claims is respectfully requested.

II. Amendments To The Claims

Claims 3, 5, 6, 8, 10, 11, 13, and 14 have been amended for reasons of clarity and not to distinguish over the cited references. Claim 3 has been amended to clarify that "said set of exception registers is for servicing exceptions having a high priority not for those exceptions having a low priority." Claims 5, 6, and 8 have been amended to depend from now independent Claim 2, as previously they were dependent on cancelled Claim 1. Claims 10, 11, and 14 have been amended to depend from now independent Claim 12, as previously they were dependent on cancelled Claim 9. Claim 13 has been amended to depend from new Claim 21. None of the amendments to the claims narrow the scope of the claims.

III. Claim Rejections Under 35 U.S.C. § 102(e)

a. Claims 1-4 and 6-8

Claims 1-4 and 6-8 are rejected under 35 U.S.C. § 102(e) as being anticipated by Yoshioka et al. (U.S. Patent No. 6,425,039). Claim 1 has been cancelled and the rejection with respect to Claim 1 is now moot.

Yoshioka et al. disclose that "general-purpose registers R0 to R7 are provided in two sets, i.e., banks 0 and banks 1." (Col. 9, ll. 56-57). Bank 0 "pertain[s] to a first general-purpose register set and Bank 1 "pertain[s] to a second general-purpose register set." (Col. 9, ll. 57-60). Further, "in the user stage shown in FIG. 4, general-purpose registers R0 (BANK0) of bank 0 are utilizable," however, "[i]n the supervisor state, the mode for utilizing the general-purpose registers R0 to R7 are determined depending upon the state of setting register bank bits RB (SR, RB) of a status register SR that will be described later." (Col. 9, ll. 67 - Col. 10, l. 6). In the "supervisor state as shown in, for example, FIG. 5, when RB=0, then, R0 (BANK0) to R7 (BANK0) are permitted to be freely used as general-purpose registers, and R0 (BANK1) to R7 (BANK1) are accessed by only the control load instruction (LDC) and the control store instruction (STC). (Col. 10, ll. 6-11). On the other hand,

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"[w]hen RB=1 ... R0 (BANK1) to R7 (BANK1) are permitted to be freely used as general-purpose registers, and R0 (BANK0) to R7 (BANK0) are accessed by only the control load instruction (LDC) and the control store instruction (STC)." (Col. 10, ll. 11-15). Therefore, Yoshioka et al. disclose one set of general registers, portions of which are used during different states of operation.

In Yoshioka et al. "[w]hen an instruction is executed like a pipe-line, a general exception event of a priority level 3 detected during the execution of a given instruction is accepted prior to other general exception events of the priority level 3 that are detected during the execution of a subsequent instruction." (Col. 13, ll. 25-30). Where, "the execution order is defining the priority order within an execution span of the individual instructions." (Col. 13, ll. 30-32). Therefore, Yoshioka et al. utilizes priorities to handle the order of interrupt processing. However, all interrupts are processed utilizing the same method.

Claim 2, recites, *inter alia*, "a set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers when an exception occurs, wherein said set of exception registers is substantially dedicated for servicing exceptions." Yoshioka et al. disclose utilizing general purpose registers that are used both for exception handling and user processing, not "a set of dedicated exception registers" that are "substantially dedicated for servicing exceptions." Therefore, Claim 2 is allowable for at least this reason.

Claims 3-4 and 6-8 depend from Claim 2 and are therefore allowable over Yoshioka et al. for at least the same reason as stated with respect to Claim 2.

Moreover, Claim 3 recites "wherein said set of exception registers is for servicing exceptions having a high priority not for those exceptions having a low priority," which is not taught or disclosed by Yoshioka et al. Therefore, Claim 3 is allowable over Yoshioka et al. for at least this reason.

b. Claims 9-14 and 16-18

Claims 9-14 and 16-18 are rejected under 35 U.S.C. § 102(e) as being anticipated by Yoshioka et al. (U.S. Patent No. 6,038,661). Claims 9 and 16 are being cancelled and the rejections with respect to Claims 9 and 16 are now moot.

Claim 12 recites, *inter alia*, "servicing said exception using said at least one set of exception registers if said exception is a high priority exception," and "preserving information from the set of general purpose registers in a memory if said exception is a low priority exception." Yoshioka et al. disclose that "the execution order is defining the priority order

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within an execution span of the individual instructions." (Col. 13, ll. 20-22). Yoshioka et al. utilize priorities to handle the order of interrupt processing, where all interrupts are processed utilizing the same set of registers. Claim 12 is therefore allowable for at least this reason.

Claims 10, 11, 13-15 and 19 depend from Claim 12 and are therefore allowable over Yoshioka et al. for at least the same reason as stated with respect to Claim 12.

Moreover, Claim 19 recites, *inter alia*, "wherein said providing comprises providing a second vector and not activating said set of exception registers for lower priority exceptions." Yoshioka et al. disclose that all interrupts are processed utilizing the same set of registers and does not disclose "not activating said set of exception registers for lower priority exceptions." Claim 19 is therefore allowable for at least this reason.

Claim 13 depends from Claim 19 and is therefore allowable over Yoshioka et al. for at least the same reason as stated with respect to Claim 19.

Claim 17 recites, *inter alia,* "means for servicing said ... including means for activating at least one set of dedicated exception registers." Yoshioka et al. disclose "general-purpose registers R0 to R7 are provided in two sets, i.e., banks 0 and banks 1." (Col. 9, ll. 48-50). Yoshioka et al. disclose one set of general registers, portions of which are used during different states of operation. Therefore, Claim 17 is allowable for at least this reason.

Claim 18 depends from Claim 17 and is therefore allowable over Yoshioka et al. for at least the same reason as Claim 17.

Moreover Claim 18 recites "means for activating comprises ... a second select logic circuit coupled to said at least one set of exception registers, said second select logic circuit receives an execution register active bit enabling said at least one set of exception registers and said second select logic circuit receives an inverted execution register active bit disabling said set of general purpose registers." This recitation is not taught or disclosed by Yoshioka et al., which disclose using address offsets for selecting registers for certain types of exceptions, but not the use of "an execution register active bit enabling said at least one set of exception registers" and "an inverted execution register active bit disabling said set of general purpose registers." Therefore, Claim 18 is allowable for at least this reason.

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IV. Claim Rejections Under 35 U.S.C. § 103(a)

a. Claim 5

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshioka et al. (U.S. Patent No. 6,425,039).

Claim 5 depends from Claim 2 and is therefore allowable for at least the same reason as Claim 2.

b. Claims 13-15

Claims 13-15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshioka et al. (U.S. Patent No. 6,038,661).

Claims 13-15 depend from Claim 12 and are therefore allowable for the same reason as stated with respect to Claim 12.

V. New Claims

New Claims 19-24 are fully supported by the specification, add no new matter, and contain limitations not taught or disclosed in Yoshioka et al. As such, Applicants respectfully submit that Claims 19-24 are allowable.

Conclusion

For the above reasons, Applicants respectfully request allowance of Claims 2-8 and 10-24. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 453-9200, extension 1338.

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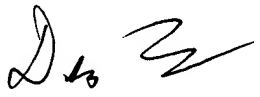
Respectfully submitted,



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Version with markings to show changes made

In the Claims

Please amend Claims 2, 3, 5, 6, 8, 10-14 and 17 as follows.

2. (Amended) A processor comprising:

a set of general purpose registers; and

a set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers when an exception occurs, [The processor of Claim 1,] wherein said set of exception registers is [a] substantially dedicated [set of registers] for servicing exceptions.

3. (Amended) The processor of Claim 2, wherein said set of exception registers is for servicing exceptions having a high priority not for those exceptions having a low priority.

5. (Amended) The processor of Claim [1]2, wherein there are at least eight exception registers.

6. (Amended) The processor of Claim [1]2, wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls.

8. (Amended) The processor of Claim [1]2, further comprising:

a select logic circuit having a first input terminal that receives an exception register active bit and a second input terminal that receives a register address bit, said select logic circuit provides an output signal on an output terminal used to select between said set of general purpose registers and said exception registers.

10. (Amended) The method of Claim 12[9], wherein said at least one set of exception registers is a dedicated set of exception registers.

11. (Amended) The method of Claim 12[9], wherein servicing said exception using said at least one set of exception registers comprises modifying the values of the registers in said set of exception registers without disrupting the state of the interrupted task.

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12. (Amended) A method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

swapping a set of general purpose registers for at least one set of exception registers [The method of Claim 9, wherein] if an exception asserted at said processor is a high priority exception; [, said method further comprising:]

servicing said exception using said at least one set of exception registers if said exception is a high priority exception;

preserving information in the set of general purpose registers in a memory if said exception is a low priority exception; and

swapping out said exception registers for said set of general purpose registers and resuming execution of said task if said exception is a high priority exception.

[providing a first vector and activating said at least one set of exception registers for said high priority exception; and]

providing a second vector and not activating said set of exception registers for lower priority exceptions.]

13. (Amended) The method of Claim 19[12], wherein said first vector is a dedicated vector and said providing said first vector automatically separates said high priority exception from said lower priority exceptions.

14. (Amended) The method of Claim 12[9], wherein said exception is a high priority exception and is either an interrupt or an operating system call, said method further comprising:

providing a first vector and activating at least a portion of said exception registers for said high priority exception when said exception is an interrupt;

providing a second vector and activating at least another portion of said exception registers for said high priority exception when said exception is an operating system call; and

providing a third vector and not activating said set of exception registers for lower priority exceptions.

17. (Amended) [The apparatus of Claim 16, wherein:] An apparatus for executing tasks and servicing exceptions, said apparatus comprising:

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means for interrupting a task when an exception is asserted;

means for servicing said exception without disrupting the state of the interrupted task, including [said means for servicing comprises a] means for activating at least one set of dedicated exception registers; and

means for resuming execution of said interrupted task, including [means for resuming execution of said interrupted task comprises a] means for deactivating said dedicated exception registers and activating general purpose registers to resume execution of said task.

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